ULTRA-FAST IMAGE BASED CONTROL

Euresys Custom Logic for FPGAs enables Machine Learning based processing at the edge

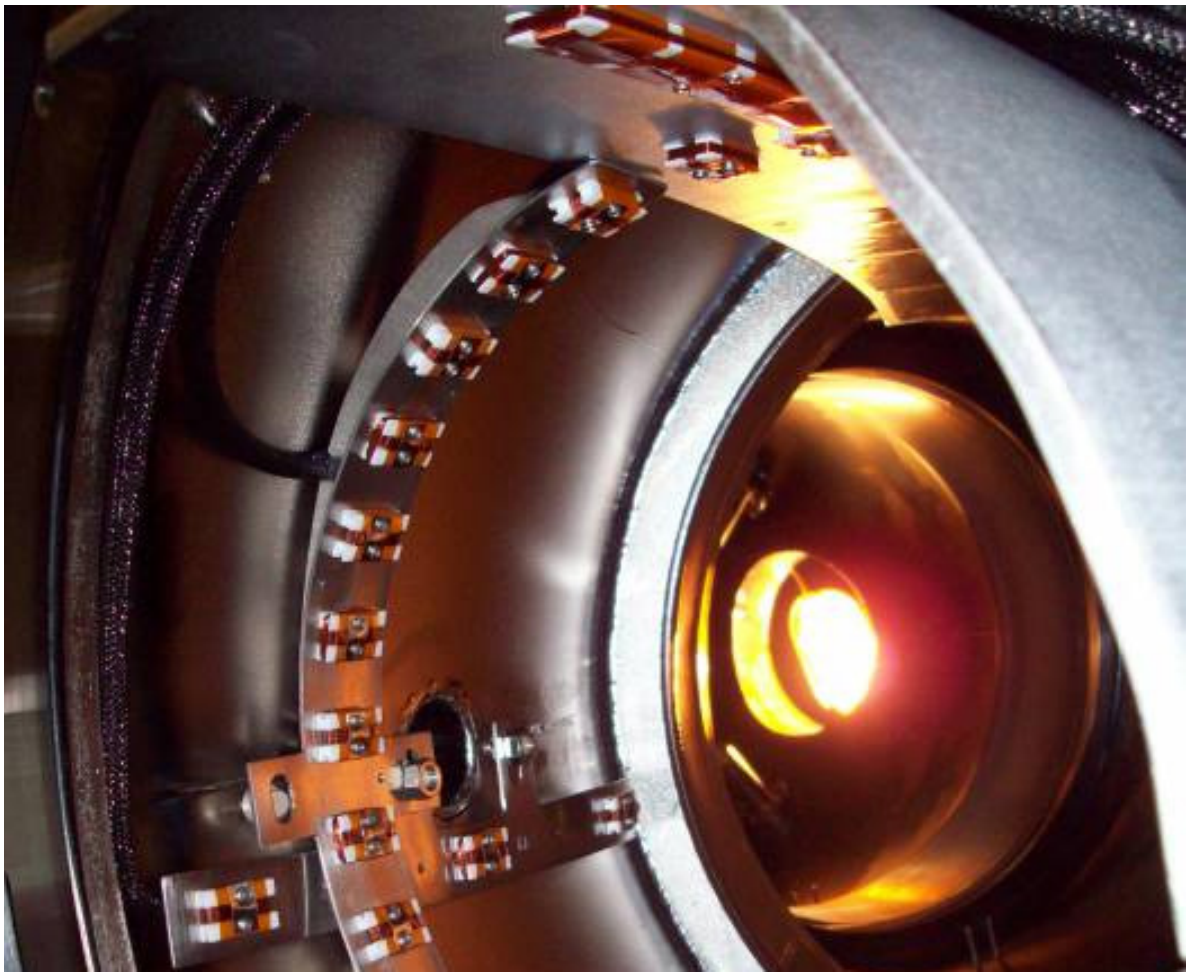

FIGURE 1 - *Peeking inside the Columbia HBT-EP Tokamak - © J. Levesque*

Euresys frame grabbers and their CustomLogic capability have enabled a team of researchers from Columbia University, Drexel University, Fermilab, and Lehigh University to develop new capabilities for fusion energy by greatly reducing the time between signal acquisition and control command in a camera-based high-speed tokamak plasma control loop.

In this new example of “Vision-in-the-Loop”, plasma control requirements reach unprecedented speed for such complex control logic.

THE APPLICATION

A tokamak, such as the one in Figure 2, is a machine that confines a high-temperature plasma using magnetic fields in a donut shape which scientists refer to as a torus. “Fusion energy scientists believe that tokamaks are currently one of the leading plasma confinement concepts for future fusion power plants”[i].

Active feedback control in magnetic confinement fusion devices is desirable to mitigate plasma instabilities and enable robust, high-performance operation. Optical high-speed cameras provide a powerful, non-invasive diagnostic and can be suitable for these applications.

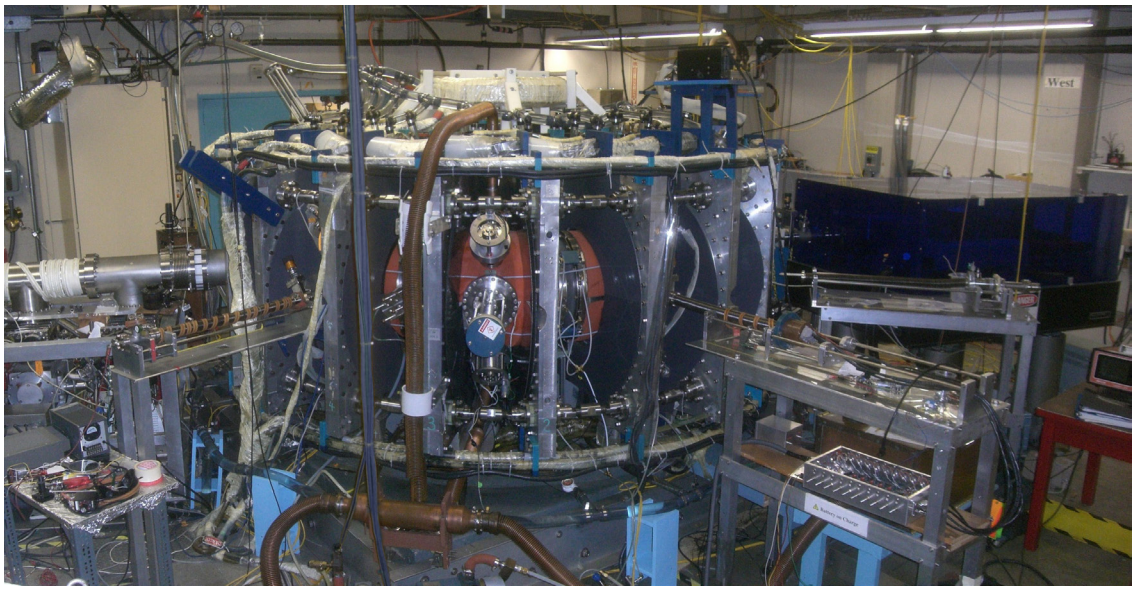

FIGURE 2 - *Columbia HBT-EP Tokamak - © D. Shiraki*

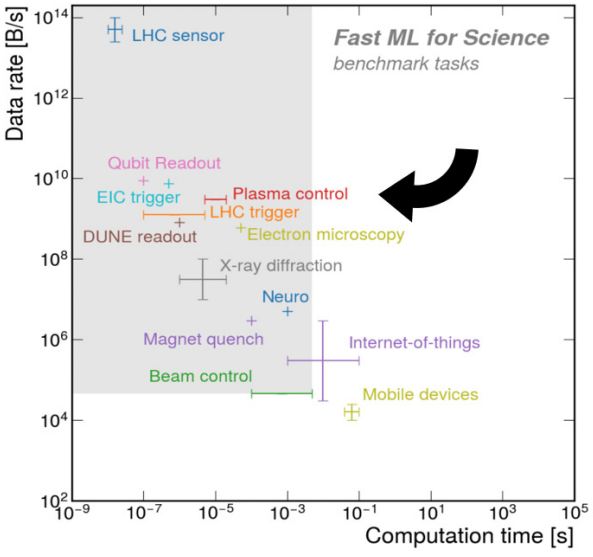

FIGURE 3 - *Data rate versus Computation time of various processes - Fast ML for Science - © N. Tran*

In their paper, the research team described how they processed fast camera data, at rates exceeding 100,000 fps, on in-situ Field Programmable Gate Array (FPGA) hardware for plasma control at the HBT-EP fusion experiment at Columbia University. The purpose is to track magnetohydrodynamic (MHD) instability evolution and generate control requests in real-time (See Figures 3 & 4). To achieve that, the team implemented a Convolutional Neural Network (CNN) model on the frame grabber’s built-in FPGA, allowing them to achieve a trigger-to-output latency of 17.6 µs and throughput up to 120,000 fps.

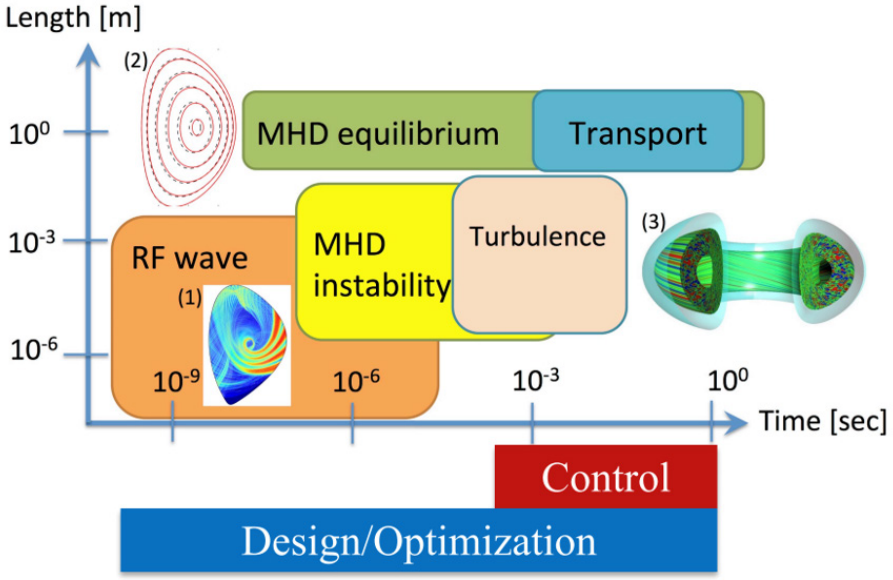

FIGURE 4 - *Time and length scales of magnetohydrodynamics (MHD) instabilities, in addition to other plasma phenomena that require optimization or real-time control – Fermilab & Columbia University FastML Workshop 09_26_2023 © C. Hansen*

THE SELECTED SOLUTION

The hardware platform consisted of:

- The AMETEK Phantom S710™ camera (Up to 7 Gpx/second (87.5 Gbps) of streaming capability e.g. 7,275 fps at 1,280 x 800,
- Euresys Coaxlink Octo frame grabber accommodating outputs of the camera.

In this case, channeling the data to a CPU, or even GPU, for central processing would not have met the responsiveness requirements of the application, which are in the 10 µs range.

The possibility of using Euresys' CustomLogic offered researchers the unique opportunity of programming their own plasma control algorithms (CNN inference) directly in the Coaxlink Octo frame grabber to achieve latencies commensurate with the plasma dynamics.

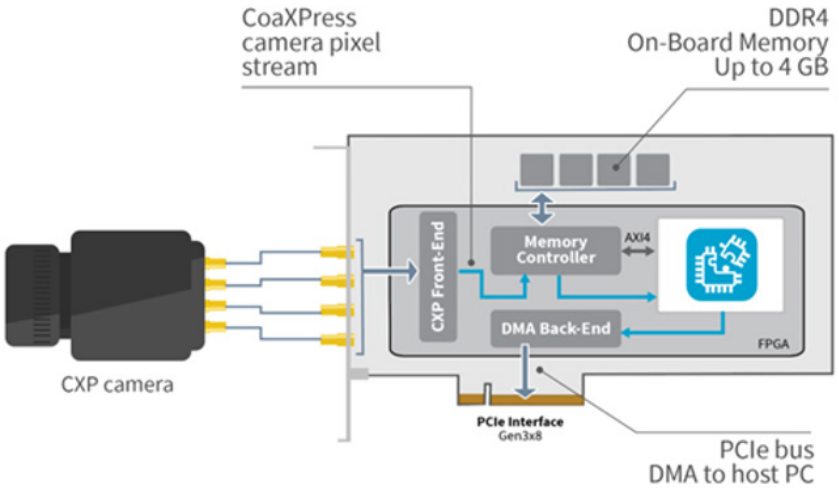

FIGURE 5 - *Euresys Coaxlink Quad frame grabber's CutomLogic capability - © Euresys*

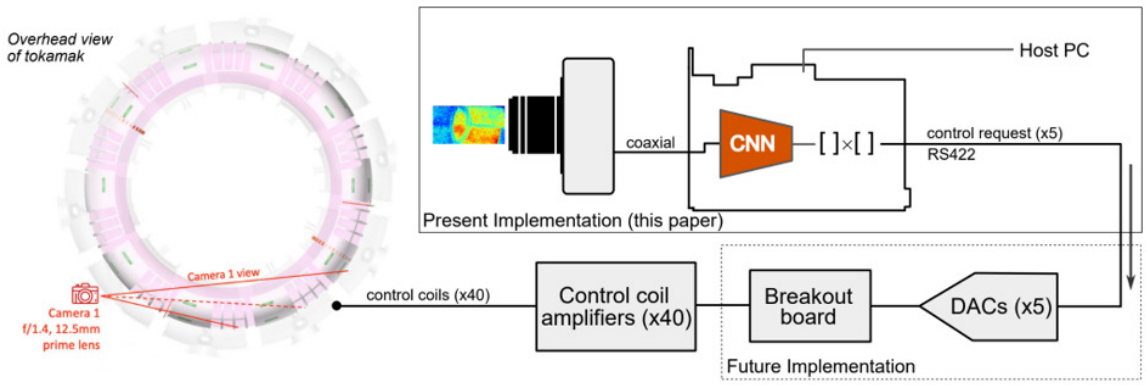

FIGURE 6 - *Tokamak magnetic confinement closed loop controlii - © R. Forelli* [ii]

Programming the Coaxlink CustomLogic can be done using AMD Vivado™ development tools. The FPGA resources are allocated for three main usages:

- The CoaXPress protocol,
- The internal card management,
- The user defined CustomLogic, in this instance the Neural Network model of the control algorithm and the control output request computation.

The team took on the challenge of implementing a more powerful control algorithm than usual while meeting the resource constraints of the frame grabber FPGA chip. To this end, they have used the open-source High-Level Synthesis for Machine Learning (hs4ml)[iii] package to translate and optimize the model before synthesizing and deploying it to the frame grabber's FPGA.

The Coaxlink Octo I/Os interface directly with the plasma control system (external hardware in development), and image data are transferred to the host computer via the PCIe bus for post-processing outside of the control loop.

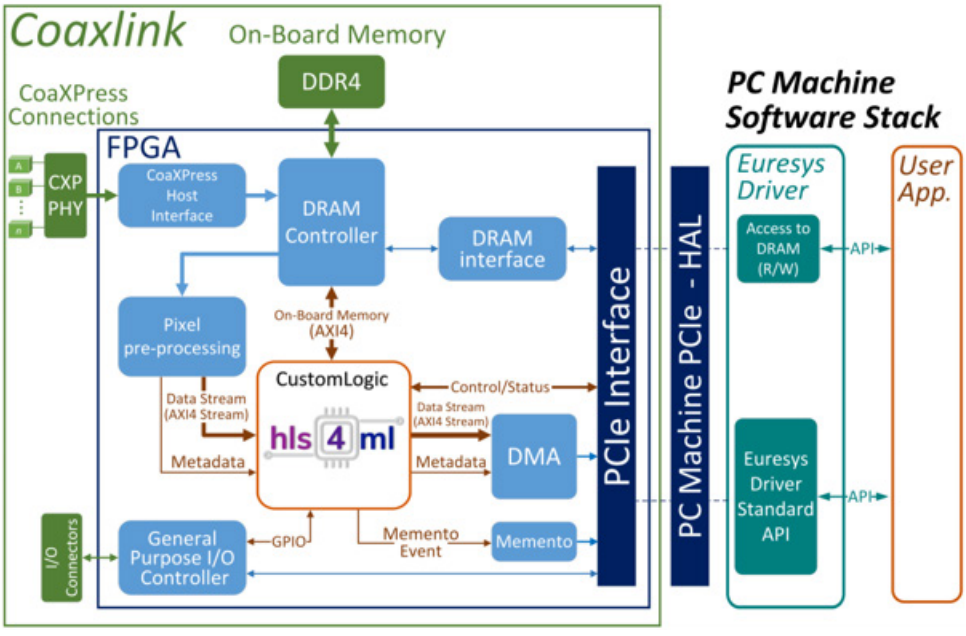

FIGURE 7 - *Implementation of hls4ml in Euresys CustomLogic*[iv] *- © R. Forelli*

The implementation ultimately achieved a latency of 7.7 µs for the CNN model itself, 17.6 µs total for the acquisition trigger to output control request, and is able to run at pipelined frame rates of up to 120 kfps, meeting the requirements for real-time control of MHD instabilities in the tokamak.

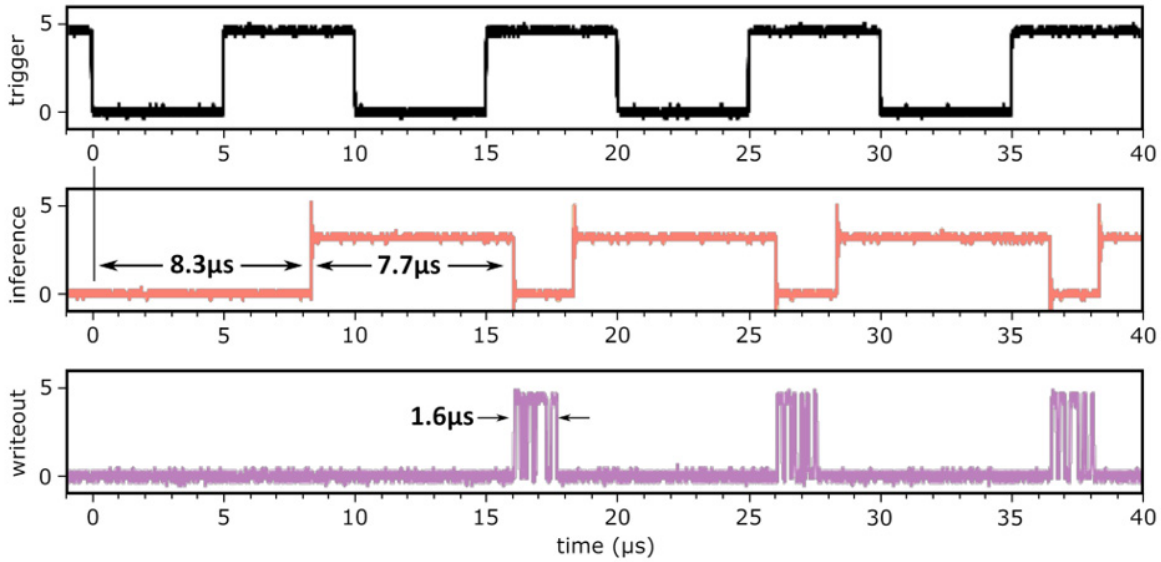

FIGURE 8 - *Oscilloscope timing diagram indicating achieved latency. Acquired using Euresys Octo GPIO - © Y. Wei* [ii]

THE TOOLKITS

In addition to AMD Vivado™ tools, the developers are extensively assisted by additional Euresys tools such as:

- General Purpose I/O Interface, enabling easy benchmarking of firmware model latency and throughput via 10MHz RS422 differential IO (shown above).
- Memento Event Logging Tool, providing a precise timeline of time-stamped events, along with context information and logic analyzer view. A valuable assistance during application development and debugging.
- Control/Status interface, allowing the user to read and write registers inside the user logic via the Coaxlink Driver API.
- The Reference Design delivered with the Coaxlink CustomLogic SDK and intended to be used as a template. The reference design exposes all interfaces available to the user.

CONCLUSION

This specific implementation of CustomLogic illustrates how Euresys solutions provide access to cutting-edge image processing for researchers to implement their own custom algorithms.

By allowing third parties to implement a low level fast running custom logic at the FPGA level (instead of CPU/GPU based higher level programming), the Coaxlink frame grabber allows users to cope with demanding process control timing constraints.

This could be true in many other time-constrained application areas, beyond that specifically discussed here.

Each time a bottleneck is removed in a chained process, it opens the way to a realm of newer, and often more demanding, applications and specifications. And Euresys is already paving the way to allow even more precise control by accommodating higher capacities over copper or fiber connectivity. And image transmission/processing links, like those offered by Euresys, will meet these requirements by offering even higher capacities over copper or fiber connectivity.

Further information about the project can be found on the ArXivportal
https://arxiv.org/abs/2312.00128
as well as an intro tutorial about the implementation on GitHub.

Further information about the Euresys frame grabbers and CustomLogic can be found here:
https://www.euresys.com/en/Products/Frame-Grabbers/Coaxlink-series

[i] US Department Of Energy (DOE) Office of Science

[ii] Low latency optical-based mode tracking with machine learning deployed on FPGAs on a tokamak [Y. Wei, R. F.Forelli, C. Hansen, J. P. Levesque, N. Tran, J. C. Agar, G. Di Guglielmo, M. E.Mauel, and G. A. Navratil]

[iii] Welcome to hls4ml's documentation! — hls4ml 0.8.1 documentation (fastmachinelearning.org)

[iv] Euresys, D209ET-Coaxlink CustomLogic User Guide-eGrabber 16.0.2.2128, Euresys S.A., Seraing, Belgium (2021)